WHAT IS CLAIMED IS:

1. A semiconductor chip package, comprising:

a semiconductor chip which includes a through hole extending there through from an active first surface to an inactive second surface;

a first conductive pad which at least partially surrounds the through hole on the active first surface of the semiconductor chip;

a printed circuit board which includes a first surface attached to the inactive second surface of the semiconductor chip, and which further includes a second conductive pad aligned with the through hole of the semiconductor chip; and

a conductive material which fills the through hole and contacts the first and second conductive pads.

2. A semiconductor chip package as claimed in claim 1, wherein the conductive material comprises solder.

3. A semiconductor chip package as claimed in claim 2, wherein the solder forms a solder bump over the active first surface of the semiconductor chip.

4. A semiconductor chip package as claimed in claim 1, wherein the conductive material comprises a metal plug

which protrudes into the through hole from the second conductive pad of the printed circuit board, and solder which surrounds the metal plug.

5. A semiconductor chip package as claimed in claim 4, wherein the solder forms a solder bump over the active first surface of the semiconductor chip.

6. A semiconductor chip package as claimed in claim 1, wherein the printed circuit board includes an aperture aligned below the second conductive pad opposite the through hole.

7. A semiconductor chip package as claimed in claim 4, further comprising an electrode which is electrically connected to the second conductive pad and which protrudes through the aperture in the printed circuit board.

8. A semiconductor chip package as claimed in claim 7, wherein the electrode is a solder ball.

9. A semiconductor chip package as claimed in claim 1, further comprising an electrode which is electrically connected the second conductive pad and which is attached

to a second surface of the printed circuit board opposite the first surface of the printed circuit board.

10. A semiconductor chip package as claimed in claim 9, wherein the electrode is a solder ball.

11. A semiconductor chip package as claimed in claim 1, further comprising an insulating layer located on sidewalls of the through hole of the semiconductor chip.

12. A semiconductor chip package as claimed in claim 1, further comprising an adhesive layer interposed between the inactive second surface of the semiconductor chip and the first surface of the printed circuit board.

13. A semiconductor chip package as claimed in claim 1, further comprising an anisotropic conductive film interposed between the inactive second surface of the semiconductor chip and the first surface of the printed circuit board.

14. A semiconductor chip package as claimed in claim 1, further comprising a protective layer covering the active first surface of the semiconductor chip.

15. A semiconductor multi-package stack, comprising:

a plurality of stacked semiconductor chip packages, each chip package comprising (a) a semiconductor chip which includes a through hole extending there through from an active first surface to an inactive second surface, (b) a first conductive pad which at least partially surrounds the through hole on the active first surface of the semiconductor chip, (c) a printed circuit board which includes a first surface attached to the second surface of the semiconductor chip, and a second conductive pad which is aligned with the through hole of the semiconductor chip, and (d) a conductive material which fills the through hole and contacts the first and second conductive pads.

16. A semiconductor multi-package stack as claimed in claim 15, wherein the semiconductor chip packages are stacked such that the conductive material of a lower chip package contacts the printed circuit board of an adjacent upper chip package.

17. A semiconductor multi-package stack as claimed in claim 16, wherein the conductive material of each semiconductor chip package comprises solder.

18. A semiconductor multi-package stack as claimed in claim 17, wherein the solder forms a solder bump over the active first surface of the semiconductor chip of each semiconductor chip package.

19. A semiconductor multi-package stack as claimed in claim 18, wherein the conductive material of each semiconductor chip package comprises a metal plug which protrudes into the through hole from the second conductive pad of the printed circuit board, and solder which surrounds the metal plug.

20. A semiconductor multi-package stack as claimed in claim 19, wherein the solder forms a solder bump over the active first surface of the semiconductor chip of each semiconductor chip package.

21. A semiconductor multi-package stack as claimed in claim 16, wherein the printed circuit board of each semiconductor chip package includes an aperture aligned below the second conductive pad opposite the through hole, and wherein the conductive material of the lower chip package contacts the second conductive pad of the printed

circuit board of the adjacent upper chip package through the aperture of the adjacent upper chip package.

22. A semiconductor multi-package stack as claimed in claim 16, further comprising an electrode which is electrically connected to the second conductive pad a lowermost semiconductor chip package and which protrudes through the aperture in the printed circuit board of the lowermost semiconductor chip package.

23. A semiconductor multi-package stack as claimed in claim 16, wherein the electrode is a solder ball.

24. A semiconductor multi-package stack as claimed in claim 16, further comprising an electrode which is electrically connected the second conductive pad of the lowermost semiconductor chip package of the and which is attached to a second surface of the printed circuit board opposite the first surface of the printed circuit board.

25. A semiconductor multi-package stack as claimed in claim 24, wherein the electrode is a solder ball.

26. A semiconductor chip package as claimed in claim 16, further comprising an insulating layer located

on sidewalls of the through hole of the semiconductor chip of each semiconductor chip package.

27. A semiconductor chip package as claimed in claim 16, further comprising an adhesive layer interposed between the inactive second surface of the semiconductor chip and the first surface of the printed circuit board of each semiconductor chip package.

28. A semiconductor chip package as claimed in claim 16, further comprising an anisotropic conductive film interposed between the inactive second surface of the semiconductor chip and the first surface of the printed circuit board of each semiconductor chip package.

29. A semiconductor chip package as claimed in claim 16, further comprising a protective layer covering the active first surface of the semiconductor chip of an uppermost semiconductor chip package.

30. A semiconductor multi-package stack as claimed in claim 15, wherein the semiconductor chip packages are stacked such that the conductive material of an upper chip package contacts the printed circuit board of an adjacent lower chip package.

31. A semiconductor multi-package stack as claimed in claim 30, further comprising an external printed circuit board having a first conductive pad formed on a first surface and a second conductive pad formed on an opposite second surface, and further having an external electrode attached to the second conductive pad, wherein the conductive material of the bottommost semiconductor chip package is attached to the first conductive pad of the external printed circuit board, and wherein the first and second conductive pads of the external printed circuit board are electrically connected.

32. A semiconductor multi-package stack as claimed in claim 31, wherein the external electrode is a solder ball.

33. A method for manufacturing a semiconductor chip package, said method comprising:

forming a through hole through a semiconductor chip, the through hole extending from an active first surface of the semiconductor chip to an opposite inactive second surface of the semiconductor chip, wherein a first conductive pad at least partially surrounds the through hole on the first surface of the semiconductor chip;

attaching a first surface of a printed circuit board to the second surface of the chip such that a second conductive pad of the printed circuit board is aligned with the through hole of the semiconductor chip; and

filling the through hole with a conductive material such that the conductive material contacts the first and second conductive pads.

34. The method as claimed in claim 33, further comprising forming a metal plug which protrudes from the second conductive pad, and inserting the metal plug into the through hole of the semiconductor chip upon attachment of the first surface of the printed circuit board to the second surface of the semiconductor chip.

35. The method as claimed in claim 33, wherein the first conductive pad is formed on the active first surface of the chip prior to formation of the through hole, and wherein through hole is formed through the first conductive pad such that a remaining portion of the first conductive pad at least partially surrounds the through hole.

36. The method as claimed in claim 33, wherein said formation of the through hole comprises:

forming a trench in the first surface of the semiconductor chip;

depositing an insulating layer at least on side walls of the trench; and

removing a surface portion of the second surface of the semiconductor chip to expose the trench.

37. The method as claimed in claim 36, wherein the surface portion of the second surface of the semiconductor chip is removed by mechanical grinding.

38. The method as claimed in claim 36, wherein the surface portion of the second surface of the semiconductor chip is removed by chemical mechanical polishing.

39. The method as claimed in claim 33, wherein the first surface of the printed circuit board is attached to the second surface of the semiconductor chip using an adhesive.

40. The method as claimed in claim 33, wherein the first surface of the printed circuit board is attached to the second surface of the semiconductor chip using an anisotropic conductive film.

41. The method as claimed in claim 33, wherein the conductive material electrically contacts the second conductive pad through the anisotropic conductive film.

42. A method of manufacturing a semiconductor chip package, said method comprising:

forming a plurality of through holes through a respective plurality of semiconductor chips contained in a wafer, the through holes extending from an active first surface of the wafer to an opposite inactive second surface of the wafer, wherein a first conductive pad at least partially surrounds each through hole on the first surface of the wafer;

forming a plurality of second conductive pads on a first surface a printed circuit board;

attaching the first surface of a printed circuit board to the second surface of the wafer such that the plurality of second conductive pads are respectively aligned with the plurality of through holes; and

filling the plurality of through holes with a conductive material such that the conductive material contacts the first and second conductive pads of each through hole.

43. The method as claimed in claim 42, further comprising dicing the wafer, with the printed circuit board attached thereto, into a plurality of semiconductor chip packages.

44. The method as claimed in claim 42, wherein said formation of the through hole comprises:

forming a trench in the first surface of each semiconductor chip of the wafer;

depositing an insulating layer at least on side walls of the trench of each semiconductor chip of the wafer; and

removing a surface portion of the second surface of the wafer to expose the trench of each semiconductor chip of the wafer.

45. The method as claimed in claim 44, wherein the surface portion of the second surface of the wafer is removed by mechanical grinding.

46. The method as claimed in claim 44, wherein the surface portion of the second surface of the wafer is removed by chemical mechanical polishing.

47. The method as claimed in claim 42, wherein the first surface of the printed circuit board is attached to the second surface of the wafer using an adhesive.

48. The method as claimed in claim 42, wherein the first surface of the printed circuit board is attached to the second surface of the wafer using an anisotropic conductive film.